28.8 Performance Variations of a 66GHz Static CML Divider in 90nm CMOS

Jean-Olivier Plouchart[1], Jonghae Kim[1], Victor Karam[2], Robert Trzcinski[1], Jeff Gross[1]

[1]IBM, Hopewell Junction, NY
[2]Carleton University, Ottawa, Canada

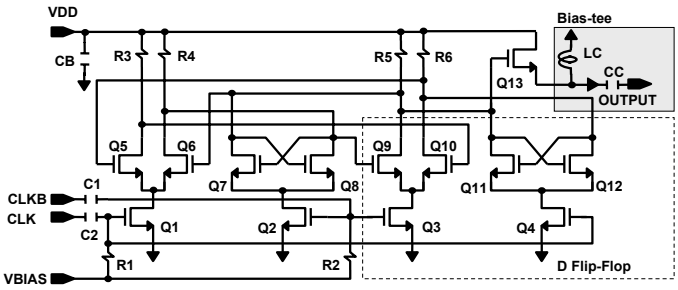
A 66GHz maximum operating clock frequency, f_{max}, is achieved by a static current-mode logic (CML) divide-by-two circuit that dissipates 25.5mW per latch and is integrated in a 90nm digital SOI CMOS technology. Statistical high-frequency measurements were performed to quantify the performance variations of such a process sensitive mm-wave nanometer-technology circuit.

With a measured f_t of more than 300GHz [1], CMOS technology will expand from RF to mm-wave applications. The CML static latch is critical for broadband applications and usually limits system performance. The first mm-wave CMOS static divider was reported in [2]. However since process tolerances do not scale for nanometer technologies, significant circuit performance variations are expected. We measure and quantify the statistical circuit performance variations based on more than 10,000 high-frequency measurements.

Figure 28.8.1 shows the block diagram of the 2:1 static frequency divider. It is based on CML master-slave latches (MSFF) connected in series. All the signals are differential, although the latches also function with a single-ended clock, since the clock common-mode level is set through the resistors $R1$ and $R2$. It can be shown that the cross connection between the output of the slave latch and the input of the master causes the clock frequency to be divided by two. The output buffer is a common-source FET biased through an external bias Tee, where the buffer current consumption can be monitored separately. A deep understanding of technology, modeling and layout optimization is required to leverage the raw speed of the technology [3]. The layout of the FET devices is especially critical to achieve the best trade-off between minimizing the FET external parasitic capacitance and resistance and optimizing the FET-channel mechanical stress [3]. S-parameter measurements indicate that a finger width of 1.89µm achieves the best trade-off between f_t and f_{max} [1]. Following circuit optimization, the total widths of the clock and data differential-pair NFETs were set to 18.9µm and 15.12µm, respectively. Even though low-V_t NFETs are available in the technology, regular-V_t NFETs were used because of their better intrinsic matching. Poly-silicon resistor loads of 75Ω were used in the latches, resulting in a 700mV$_{pp}$ voltage swing. No inductive peaking was used to extend the bandwidth. The biasing and bypass capacitors are interdigitated metal fringe capacitors. The bypass capacitor geometry was optimized to handle the millimeter-wave clock. Figure 28.8.2 shows the broadband input sensitivity with a measured minimum operating frequency of 5GHz, and a maximum operating frequency of 66GHz with 25.5mW dissipated in each latch. The circuit maximum operating frequency is increased by 2 to 2.4× over 120nm SOI and bulk CMOS designs respectively [2] [4] [5], owing to circuit, layout parasitic and technology optimization. A minimum input sensitivity is achieved at 48GHz, which is equivalent to a 24GHz output self oscillation frequency (Of_{osc}). For functional yield and performance variation analysis, one of the critical circuit performance parameters is the maximum operating frequency of the product. This is a difficult measurement because it requires a mm-wave frequency sweep and detecting proper operation of the divider. A more efficient way is to measure the CML divider output self-oscillation frequency (Of_{osc}). The maximum operating frequency (f_{max}) can be derived from the sensitivity graph, where a 37.5% delta is measured between the input-referred f_{osc} (If_{osc} =$2Of_{osc}$) and f_{max}. This measurement technique was used to quantify the circuit performance variations, and as shown in Fig. 28.8.3, Of_{osc} is between 19.4 and 25.1GHz for V_{bias} = 0.8V and V_{DD} = 1.4V. However in a SoC product the voltage supply can vary by at least ±10%, therefore the performance variation must be quantified across voltage variations. Figure 28.8.4 shows power and If_{osc} across a voltage supply variation from 0.8 to 1.8V and for each V_{DD}, V_{bias} is varied from 0.7 to 0.9V. As V_{DD} varies from 1.1 to 1.8V, the minimum and maximum values of If_{osc} vary by <1GHz, but as V_{DD} drops from 1.1 to 0.9V, the maximum value of If_{osc} drops from 47 to 39GHz. Also, only 87.8 and 4.7% as many chips are functional at V_{DD} = 1.1 and 0.9V, respectively, as are at V_{DD} = 1.6V. Therefore for a maximum functional yield the chip must be operated at 1.4V nominally and have a minimum supply voltage of 1.2V. Figure 28.8.5 provides a summary of all the statistical distributions for If_{osc} and the total dissipated power across voltage, temperature and fill pattern density effect. The If_{osc} distribution is log normal. The log normal distribution is asymmetrical with a long tail. Therefore, many chips have If_{osc} greater than average. For the nominal 1.4 and 0.8V V_{DD} and V_{bias} respectively, the mean If_{osc} is 42.3GHz with a 2.4GHz standard deviation. When voltage supply variations are taken into account, the mean and standard deviation increase to 42.6 and 2.8GHz respectively (Fig. 28.8.5). This slight increase demonstrates the stability of the voltage operating point. The low sensitivity to pattern density fill is also measured and the mean of If_{osc} only decreases by 1.6%, compared to regular pattern fill, when no pattern fill is used. However when the temperature is increased from 25 to 85˚C, the mean If_{osc} decreases by 8% (Fig. 28.8.5). Therefore, for the worst temperature case of 85˚C, the extrapolated statistical mean for the maximum operating divider frequency is 54GHz ($\mu_{Fmax} = 1.375If_{osc}$). One can compute from the log normal probability density function that if we set V_{bias} = 0.8V ±100mV and V_{DD} = 1.4V ±200mV, 99% of the chips can achieve f_{max} = 46.75GHz at T 85˚C, which is sufficient for OC768 applications with forward error correction. As shown in Fig. 28.8.5 the total dissipated power mean including buffer is 44.3mW for a 1.4V voltage supply, with a 2.2mW standard deviation. The free running divider output phase noise was also measured for five different chips at 1.4V voltage supply and 0.8V V_{bias}. A 30dB phase noise variation is measured at 1GHz offset (Fig. 28.8.6). It is not clear if the free running phase noise variations impact the phase noise once the CML divider is locked to the clock. As shown on the die micrograph in Fig. 28.8.7, the layout was kept as symmetric as possible by placing the latches back to back and by balancing signal line capacitive parasitics. Because many nanometer-technology parameters do not scale, a deep understanding of technology and circuit design is required to scale performances from one technology node to the other. Similarly, because of the non-scalability of some process tolerances, statistical design, measurements, and analysis is the only practical way to quantify the circuit performances.

Acknowledgements:
The authors acknowledge the SRDC Engineers, T. Sandwick, K. Warren, G. Patton and the IBM T.J. Watson Research Center for substantial contributions during various stages of this project.

References:
[1] N. Zamdmer et al., "A 243-GHz FT and 208-GHz Fmax, 90-nm SOI CMOS SoC Technology with Low-Power Millimeter-Wave Digital and RF Circuit Capability," *Digest of VLSI*, pp. 98 – 99, June, 2004.
[2] J.-O. Plouchart et al., "A 33 GHz 2:1 Static Frequency Divider in 0.12-µm SOI CMOS Operable at 2.7mW," *IEEE Radio Frequency Integrated Circuit Conference*, pp. 329–332, June, 2003.
[3] J.-O. Plouchart et al., "SOI 90-nm Ring Oscillator Sub-ps Model-Hardware Correlation and Parasitic-aware Optimization to 1.94-ps Switching Delay," *IEDM 2005*, Dec., 2005.
[4] H.-D. Wohlmuth, D. Kehrer, "A high sensitivity static 2:1 frequency divider up to 27GHz in 120nm CMOS," *ESSCIRC 2002*, pp. 823 – 826, Sept., 2002.
[5] U. Singh, M. M. Green, "High-frequency CML clock dividers in 0.13-µm CMOS operating up to 38 GHz," *IEEE Journal of Solid-State Circuits*, Volume 40, Issue 8, pp. 1658–1661, Aug., 2005.



(Q1 through Q6, Q9 and Q10 are W=18.8μm / L= 90nm. Q7, Q8, Q11, Q12 and Q13 are W = 15.12μm / L= 90nm. R1 and R2 are 3KΩ and R3, R4, R5, and R6 are 75Ω respectively. The AC-coupling capacitors, C1 and C2, are 1pF and CB is 20pF. LC and CC are a choke coil and a coupling capacitor in the bias-tee.)

Figure 28.8.1: Divider circuit schematic.

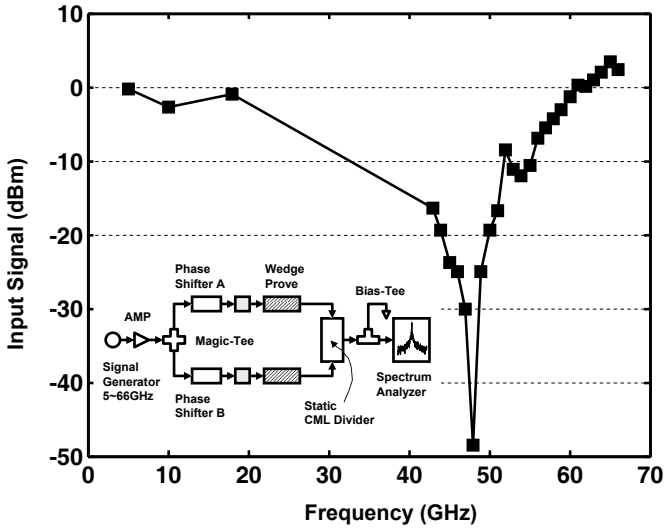


Figure 28.8.2: Broadband input sensitivity with maximum operating frequency of 66GHz.

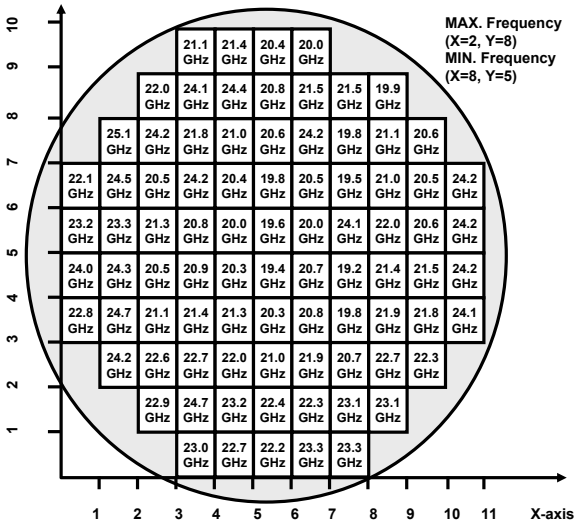


Figure 28.8.3: Output CML divider self-resonant frequency distribution across a typical wafer.

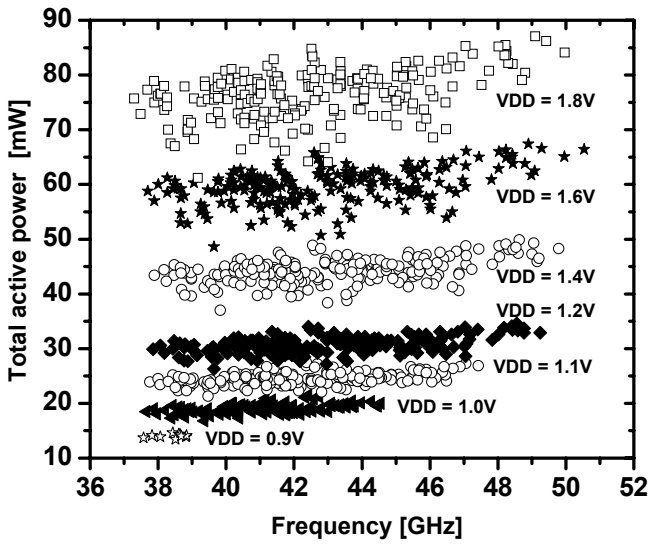


Figure 28.8.4: Power and delay statistical distribution.

Input referred (IF_{osc})	VDD=1.4V VBIAS=0.8V	VDD=(1.2, 1.6V) VBIAS=(0.7, 0.9V)	VDD=(1.2, 1.6V) VBIAS=(0.7, 0.9V) No Fill	VDD=(0.7, 0.9V) VBIAS=(0.7, 0.9V) T=85C
Probability Density Function (PDF)	Log normal	Log normal	Log Normal	Log Normal
Mean (GHz)	42.3	42.6	41.9	39.2
Standard Deviation (GHz)	2.4	2.8	2.8	2.8
Active Power Dissipation	**VDD=1.4V VBIAS=0.8V**	**VDD=1.4V VBIAS=(0.7, 0.9V)**	**VDD=1.4V VBIAS=(0.7, 0.9V) No Fill**	**VDD=1.4V VBIAS=(0.7, 0.9V) T=85C**
Probability Density Function (PDF)	Normal	Normal	Normal	Normal
Mean (mW)	44.6	44.3	44.4	41.4
Standard Deviation (mW)	1.8	2.2	2.4	1.8

Figure 28.8.5: Input-referred self-oscillation frequency and active power mean and standard deviation at T=25 and 85°C for different bias conditions.

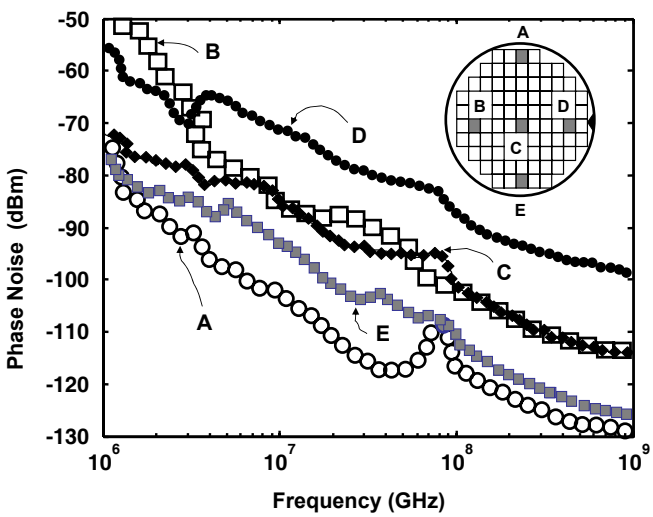
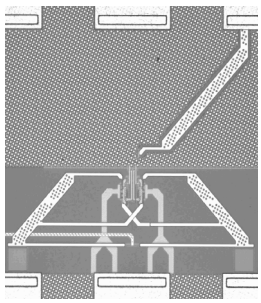
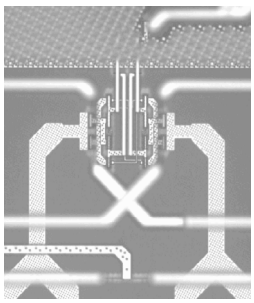


Figure 28.8.6: Output Phase noise performance from 100KHz to 1GHz offset for five sample chips.

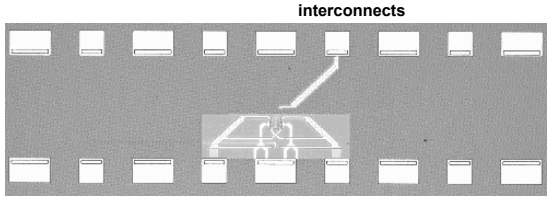
Continued on Page 671



Divider core circuit



Divider core circuit with main interconnects



Divider with wedge pad-sets (dimension: 1.3mm x 0.5mm)

Figure 28.8.7: Chip micrograph.

